REMARKS

In the Office Action, claims 1 and 8-9 were rejected under 35 USC §102(b) as being anticipated by Papaliolios. Claims 4 and 6 were rejected under 35 USC 103(a) as being unpatentable over Papaliolios in view of Jaffe et al. Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Papaliolios in view of Jaffe et al and further in view of Katti et al. Claims 2-3 were indicated to be allowable if rewritten in independent form. Claim 10 is allowed.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

The Papaliolios patent does not disclose a passive matrix memory, as is the case of the present invention. The layout of the memory device according to Papaliolios is rendered in fig. 5 wherein memory is segmented in a number of separate, but obviously, identical arrays 100, 101 each array being connected to a column or reference memory cells 106, 107. The arrays 100 and 101 are referred to as "single transistor" and it is explicitly stated in col. 2, line 59 etc. of Papaliolios "a ferroelectric memory can be realized having an array of single-transistor, single-capacitor ferroelectric memory cells..". This corresponds, of course, to an active matrix-addressable memory of the 1T-1C type, each memory

cell being connecting with the switching transistor. Also it is disclosed col. 2, line 62 etc. that the reference cells are of the 2T-2C type, i.e. with two switching transistors and two capacitors and that this indeed is the case, can be seen for instance from an inspection of fig. 6 thereof, while of course fig. 3 discloses an isolated reference memory cell. In reference memory cells the switching transistors are denoted 42 and 46 respectively and the associated capacitors 40, 44. The implication is then, of course, that several of the problems usually are associated with passive matrix-addressable memory will not necessarily be present in the embodiment of Papaliolios, as opposed to the present invention.

One of the problems the present invention aims to solve is to eliminate reference circuits or reference memory cells altogether, particularly because the use of reference cells either located in columns on the side of the memory matrix proper or even distributed randomly in a matrix of memory cells is not necessarily reliable, due to the inherent tendency to disturb voltages, sneak current and stray capacitive couplings in a passive matrix-addressable memory, wherein the memory material usually are provided as a global thin film and with all addressing electrodes directly interfacing the memory material with the word lines of course oriented orthogonal to the bit lines and the memory cell then generated in the volume between the crossings of word lines and bit lines. To this end the present invention proposes a dual

read method which can be performed on a memory cell means by two principal schemes as given in the description of the application.

The dual read method involves the use of successive reads, in the first scheme by pulsing the word line high once and performing two consecutive reads. In the other scheme the word line is pulsed high twice and a read is preformed each time. In this manner it is possible to store two binary values and obtain two differential signals by integrating a sensed charge over time. In a subsequent step of the second scheme the second integrated charge value is subtracted from the first, the difference is compared with a threshold level which is given as an offset, e.g. from a zero voltage value (usually ground), and a determination of the stored logical value either as a binary 1 or binary 0 is obtained dependent in on whether the difference between the integrated charge value is larger or smaller than the threshold value. Errors due to background current, offsets and process variations of the transistors in the integrator circuit or the sense amplifier will be constant values in the difference obtained and a cumulative error can be eliminated by adjusting the hypothetical threshold value in a correction circuit if required. The threshold value can be corrected by introducing a correction circuit in which case any errors are eliminated and the comparison is referred to as a zero voltage or floating ground. The sequential integration, i.e. the dual read on a single bit line,

allows for an embodiment with a self-referencing readout circuit as shown to advantage in fig. 4 of the present invention. To sum up, the present invention differs from Papaliolios in providing an essentially self-referencing readout method and self-referencing readout circuit based on a dual read wherein each read is performed as an integration of charge with respect to time in two different time intervals in consecutive operations. In other words the present invention entirely dispenses with the need for providing separate reference memory cells as is the case of Papaliolios, which anyway concerns an active matrix-addressable memory.

Concerning the claim rejections in view of 35 USC §103 whereby the Examiner relies on Papaliolios in view of Jaffe et al. (U.S. Patent No. 5,086,412), it should be noted that Jaffe et al. similarly to Papaliolios also concerns an active matrix-addressable memory and it is moreover explicitly stated in e.g. claim 1 that "each memory cell being selectively coupled to said corresponding bit line by an access control transistor so that only one memory cell in said column is coupled to said bit line at a time". This of course, implies that the Jaffe memory cell is of the 1T-1C type, i.e. with one transistor/one capacitor as eminently clear from an inspection of e.g. fig. 4 of Jaffe, where a memory cell 202 in any case corresponds to the memory cell 102 of prior art in fig. 1, viz. with one capacitor and one switching transistor. This also makes it easier for Jaffe et al to dispense with the need of

providing dedicated reference memory cells. According to Jaffe et al a word line, e.g. 206 is pulsed high, without connecting to the memory cell (e.g. 202), a strobe pulse on driver line 208 switches a word line select transistor and voltage signal is output on bit line 212 and sampled and stored in the first sample-and-hold circuit 220.

After returning the bit line to ground potential, the memory cell is read a second time in a similar manner and the output voltage or bit line 212 sampled and stored in a sample-and-hold circuit 222 and the logical value stored found by comparing voltage values 222 of the sample-and-hold circuits 220 and 222 in the sense amplifier 238, which determines the stored logic values, either a binary 0 and binary 1, from the output amplifier voltage differential. According to Jaffe et al. the word line is initialized to the required voltage level and remains at this level throughout the whole readout process, while two short data strobe signals on line 208 and separated by a time delay, is used for generating an output voltage signal on bit line 212.

As opposed to Jaffe et al the present invention relies on an integration of charge over time in selected timing intervals as can be seen from fig. 2 of the present application. However, this entails the use of a separate integrator circuit not found in either of the prior art references cited and allows for the integration of the charge to take place by either pulsing the word

line high once and performing actually a dual sensing operation in two timing intervals such that the dual read becomes a single read operation (because of pulsing the word line high only once), or it can be a true dual read by pulsing the word line high twice an integrating the charge over time, once more observing the appropriate timing intervals. This latter variant has the advantage of course of removing common offsets/missmatches in the two integrations.

Now, for instance combining the teaching of Papaliolios and the teaching of Jaffe et al would be of course serve to eliminate the need for separate reference memory cells in the form, but still one as opposed to the present invention is left with an active matrix-addressable memory, and neither will the resulting method be suited to errors inherent in a passive matrix-addressable memory and manifest by e.g. sneak currents disturb voltages and stray capacitances. Strobing a memory cell and sampling will not eliminate the problems inherent in readout of the passive matrix-addressable memories and would not be applicable to provide self-referencing as is the case of the present invention which as opposed to Jaffe et al relies on integrating the charge over time and introducing an adjustable threshold value for performing a comparison between the charge differential calculated in a dual read operation based on two consecutive charge integrations over time.

Based on the foregoing amendments and remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above amendments and remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph beginning on page 6, line 17, with the following rewritten paragraph.

-- fig. 1 shows the principle of dual ~~slope integration~~ read as used in the invention, --

Please replace the paragraph beginning on page 14, line 9, with the following rewritten paragraph.

-- The dual ~~slope integration~~ read particularly addresses a wide number of potential problems in ferroelectric memories with a polymer memory material. First, the comparison can be established with a margin close to zero. Consequently, in a fatigued memory cell where the charge is released at a lower level and occurs slower, the sensing device will still distinguish the state since the total charge released in a first time period is greater than that released in a subsequent (equivalent) time period. There is no need for a-priori knowledge of the level of fatigue to properly sense the memory cell value. Similarly, following imprint, the absolute magnitude of the charge released in any given first time

period is reduced due to the shift in the coercive field, but the relative value is still ordered. Again, the state of the memory cell can be determined with the dual slope integration without knowledge of the imprint magnitude. --

IN THE CLAIMS:

Please cancel claims 2 without prejudice or disclaimer.

Please amend claims 1 and 3 as follows:

1. (Twice Amended) A sensing device for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors, wherein said sensing device senses a current response corresponding to the data including a binary one or a binary zero, and performs an integration of two read values, the sensing device comprises an integrator circuit for sensing the current response as an integration of charge as a function of time in consecutive timing intervals and means for storing and comparing two ~~consecutive~~ consecutively read values of the current response, one of which is a reference value.

3. (Twice Amended) A sensing device according to claim ~~2~~ 11, wherein the integrator circuit comprises a switch connected in parallel over the capacitor.